A Direct-Digital 40 μA 100 kb/s Intracardiac Communication Receiver With 250 μs Startup Time for Low Duty-Cycle Leadless Pacemaker Synchronization

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***Abstract*—The first commercial dual-chamber leadless pacemaker (LLPM) was introduced recently. The system combines two separate implants situated in the right atrium and the right ventricle of the heart. Implant synchronization is accomplished with conductive intracardiac communication (CIC) using the myocardium and blood as transmission channel. Successful implant synchronization of this dual-chamber LLPM has been demonstrated. However, the continuously active synchronization transceivers, consuming about 800 nA, cause a 25-45% reduction in the projected device longevity. This work proposes an alternative strategy for power-optimized LLPM synchronization, which is based on synchronous duty-cycling of the transceivers and direct-digital CIC (DD-CIC). In line with this strategy, a novel low-power DD-CIC receiver for short-packet communication based on Manchester-encoded data and with fast startup time is presented. The circuit was fabricated in 180 nm CMOS technology and analyzed with respect to sensitivity, current consumption and startup time under highly duty-cycled operation. The receiver achieves a sensitivity of 81.6±7.4 μV at a data rate of 100 kb/s, with an active current consumption of 39.1±0.6 μA and a startup time below 250 μs. Operating the receiver as specified by the proposed LLPM synchronization strategy reduces the current consumption to a measured average value of 73 nA. In conclusion, this work suggests synchronous duty-cycling for CIC-based implant synchronization as a promising concept to severely reduce the current consumption of contemporary dual-chamber LLPMs. Consequently, device longevity may be increased significantly, potentially reducing the frequency of costly and complication-prone re-interventions.**

***Index Terms*—Baseband transmission, conductive intracardiac communication, I2I, implant-to-implant communication, direct-digital communication, intra-body communication, leadless CRT, leadless dual-chamber pacing, leadless pacemaker, Manchester code, synchronous duty-cycling.**

I. INTRODUCTION

CARDIAC pacemakers, with an annual global implantation rate exceeding 1 million, have been widely used in treating bradyarrhythmias for decades [1]. Recently, leadless pacemakers (LLPMs) have been introduced to alleviate the major complications associated with conventional devices, primarily related to transvenous leads and subcutaneous pocket implants for the pulse generator [2], [3]. Compared to conventional PMs, LLPMs are significantly smaller and omit the leads by integrating the electrodes for pacing and sensing into the device housing [2], [3], [4]. The miniaturized and lead-free design of LLPMs enables direct implantation into the heart with a catheter-based approach [2], [3], [4]. Studies have shown that LLPMs exhibit reduced overall complication rates for single-chamber right-ventricular pacing [4], [5]. The recent introduction of the first dual-chamber LLPM (cf. Fig. 1(a)), which can also sense and pace the right atrium, holds the promise to extend these benefits to the considerably larger patient population for which single-chamber pacing alone is not sufficient [6], [7], [8], [9]. Dual-chamber pacing provides the primary advantage to

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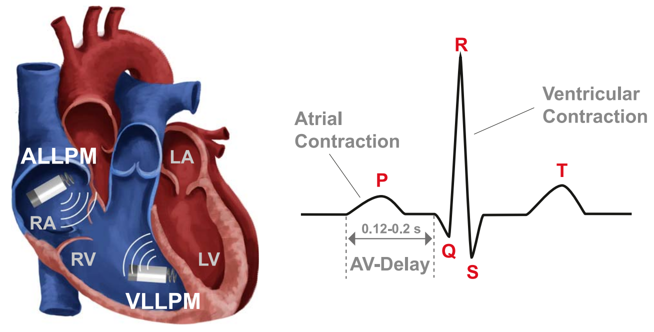


(a) (b)

Fig. 1. (a) Conceptual illustration of a dual-chamber LLPM, with one device being implanted in the right atrium (RA) and the right ventricle (RV), respectively (reprinted and adapted from [12] with permission from Elsevier). (b) Typical surface ECG waveform measured over one cardiac cycle due to the intrinsic electrical activity of the heart. In the physiological case, i.e. sinus rhythm, the P-wave precedes the QRS-complex by a time period called the AV-delay, inducing the subsequent mechanical contraction of the atrial (RA/LA) and ventricular (RV/LV) chambers.

more closely imitating natural cardiac physiology through the preservation of atrioventricular (AV)-synchrony [10]. Specifically, the LLPMs ensure that the atrial depolarization, represented by the P-wave in the ECG in Fig. 1(b), is followed by the ventricular depolarization (QRS-wave in ECG) after a set time interval known as the AV-delay. A heartbeat is typically considered as AV-synchronous if the corresponding AV-delay is less than 300 ms [8], [11]. To ensure that pacing aligns with the remaining electric activity of the heart itself, the atrial LLPM (ALLPM) and ventricular LLPM (VLLPM) use sensitive ECG sense amplifiers, which allow precise detection of the P-wave and QRS-complex, respectively [10]. Specifically, the ALLPM continuously monitors for the occurrence of intrinsic P-waves and, if none are detected, paces the right atrium to maintain a preset minimum heart rate. Each sensed or paced P-wave is then communicated by the ALLPM to the VLLPM [6]. Subsequently, the VLLPM checks for the occurrence of the corresponding intrinsic QRS-wave. If none is sensed within one AV-delay period after the P-wave, the VLLPM paces the right ventricle [6].

The LLPMs in [8] synchronize their activity using galvanic-coupled conductive intracardiac communication (CIC), a method of intra-body communication, in which the signal is conducted through the myocardium and blood. In these LLPMs, synchronization is achieved using two separate receivers; a) a low-power wake-up receiver, which is continuously running and monitoring communication attempts by the other device and b) a high-power receiver for actual data reception, which is only shortly activated upon detection of a wake-up pulse. With this dual-receiver approach, the duty-cycle of the high-power receiver can be reduced to less than 0.2%, resulting in an average current of 800 nA for synchronization per device, which is most probably dominated by the wake-up receiver [6], [13].

While achieving high AV-synchrony rates above 96% across various patient postures, the additional current consumption for synchronization considerably reduces the overall device longevity [8], [9]. In particular, when operating in synchrony with a second device, i.e. in dual-chamber mode, the ALLPM is projected to have a lifespan of only 4-6 years. This represents a 40-45% lifetime reduction compared to standalone operation, i.e. in single-chamber mode, where inter-device communication is disabled [13]. Therefore, extending battery longevity of future dual-chamber LLPMs is highly desirable from a clinical perspective. This paper focuses on reducing the current consumption of implant synchronization to address this challenge. The rest of this section reviews existing literature on LLPM synchronization and related research on low-power intra-body transceivers, circumscribes the scope of this work and outlines the subsequent sections.

A. Related Work

Various methods for synchronizing dual-chamber LLPMs have been proposed, which can be broadly grouped into two categories: indirect synchronization through an external primary device or direct implant-to-implant communication. In the first category, modalities such as radio-frequency (RF), inductive, or conductive backscatter communication have been explored for primary-to-implant communication [14], [15], [16]. Inductive communication also enables wireless power transfer, potentially extending implant longevity [15]. However, shrinking antennas to LLPM size while maintaining high power transfer efficiency remains challenging [15]. Moreover, relying on an external primary device increases the system's complexity and the risk of complications and may also compromise patient comfort. In the second category, RF communication and galvanic-coupled CIC have been extensively studied for direct implant-to-implant synchronization [6], [12], [17], [18], [19], [20], [21], [22], [23]. However, RF communication has not achieved adequately low power levels [17], [18]. This is due to the high signal absorption by the human body, combined with the use of high-frequency signals and low antenna impedance, which further increases transmitter output power [17], [18]. In contrast, CIC has been demonstrated as an energy-efficient communication method for implant synchronization. This is attributed to the moderate attenuation of the intracardiac channel, relatively high electrode impedance (typically in the range of a few hundred ohms), and the utilization of low-frequency signals (ranging from 1 kHz to 20 MHz) [6], [12], [19], [20], [21], [22], [23].

Despite these advantages of CIC, low-power LLPM synchronization remains challenging. First, both the transmitter and receiver need to operate at sub-μA current levels as they are both part of an implant with a strongly limited battery capacity. Second, given the sporadic exchange of small amounts of information, the transceivers must provide efficient short-packet communication by minimizing the number of required overhead bits for correct message detection at the receiver side. For instance, the LLPMs in [8] typically send and receive only one message with a maximum length of 32 bits per cardiac cycle (i.e. one message per second at a heart rate of 60 bpm) [6]. Thus, the synchronization transceivers need to simultaneously operate at low power levels and high energy efficiency.

Recent work on intra-body receivers based on on-off-keying (OOK) modulation operating at data rates in the range of 1–20 kHz have reported current levels of a few hundred nanoamperes [24], [25]. However, these approaches exhibit low energy-efficiency, when considering the complete communication system. In particular, their limited sensitivity would lead to an average transmitter output current significantly above 1 μA if considered in the context of LLPM synchronization with typical intracardiac attenuation and impedance levels. To improve energy efficiency, transceivers operating at substantially higher data rates based on direct-digital communication (DDC) have been proposed [26], [27], [28]. While achieving superior energy-per-bit performance, their receiver current consumption is in the range of 50–100 μA. In addition, implementations based on clock and data recovery (CDR) architectures, [26], [28], are not optimal for short-packet communication. The length of each message is considerably increased due to additional overhead bits, required by the receiver to synchronize its sampling clock to the one of the transmitter. In summary, existing intra-body receivers appear unsuitable for improving the energy-efficiency of LLPM synchronization due to high current consumption, low sensitivity levels and data overhead for packet synchronization.

Synchronous duty-cycling (SDC), wherein the receiver and the transmitter follow concurrent sleep and wake cycles, would allow to enhance sensitivity and simultaneously reduce average current consumption by minimizing idle listening time. SDC is especially promising as recent literature demonstrated that accurate timers, the main additional component required to implement the sleep/wake cycles, can be realized using 32.8 kHz quartz crystal oscillators at currents below 50 nA [29], [30], [31]. The second major determinant of the power-saving potential of SDC is the minimum achievable receiver duty-cycle, primarily limited by two factors. First, SDC introduces communication latency, necessitating careful consideration of the specific wake cycle patterns and the duration of the intervening sleep periods to ensure proper dual-chamber LLPM operation. Second, minimizing the receiver's startup phase is crucial, as current is already drained without data being received. Specifically, for SDC to be effective, the startup time must be significantly shorter than the duration of the sleep cycles. Based on the considerations outlined in this section, this article focuses on the following key aspects.

1) An alternative strategy for power-optimized LLPM synchronization is proposed, which is aimed at extending device longevity by using a single highly duty-cycled receiver, only. By restricting communication to a few periodically occurring windows per cardiac cycle, the need for continuously active wake-up receivers is eliminated and, thus, the idle time is considerably reduced.
2) The minimum required receiver duty-cycle to guarantee AV-synchrony with the proposed synchronization approach is investigated in detail based on a wake-up timer model suitable for low-power digital ASIC integration.
3) Aligned with the proposed synchronization strategy, a novel direct-digital CIC-receiver with rapid startup time is presented, which is optimized for high energy efficiency under low duty-cycle operation and sporadic short-packet communication.
4) Detailed in-silicon measurements, focusing on sensitivity, startup time, minimum duty-cycle and average current consumption, are presented for the receiver when operated as specified by the proposed synchronization strategy.

The remaining part of this paper is organized as follows: Section II presents the alternative strategy for LLPM synchronization and analyzes the minimum required receiver duty-cycle to maintain AV-synchrony. Section III provides a detailed discussion of the circuit design aspects of the proposed CIC-receiver. Subsequently, implementation results from five receiver prototype chips are presented in Section IV. The article concludes by comparing the results to previous state-of-the-art in Section V and the conclusion in Section VI.

II. SYNCHRONIZATION PROTOCOL

A. Basic Operation

Each cardiac cycle during LLPM operation is divided into two distinct phases, the alert and the refractory period (cf. Fig. 2). During the alert period, the LLPMs sense for intrinsic cardiac activity and, in absence of it, pace the heart. Subsequently, in the refractory phase immediately following ventricular excitation, both sensing and pacing circuits are disabled and, thus, no inter-device communication is required, as well. In the proposed protocol, the ALLPM and the VLLPM act as the primary and subordinate devices of the system, respectively. The ALLPM thereby controls the operation of both pacemakers as well as the synchronization process. Additionally, it is assumed that the corresponding transceivers are integrated with the remaining pacemaker circuits on the same chip. This enables the transceivers to access the output of the ECG sense amplifier and facilitates the control of the pacing unit based on received information from the second device.

As shown in Fig. 2 inter-device communication is restricted to discrete periodic windows, separated in time by t_{int}. This approach allows the transceivers to enter sleep mode between windows and consequently to reduce their power consumption.

The window timing is ensured by the ALLPM, which checks every t_{int} seconds, whether information needs to be exchanged with the VLLPM, based on any sensed/paced activity in the preceding sleep period. Specifically, as shown in Fig. 2, the ALLPM needs to send a pacing trigger and the corresponding pacing delay t_{pace} to the VLLPM in the next communication window after the detection of a P-wave. Upon successful reception of the pacing command, the VLLPM immediately sends back an acknowledge message, to which optional data for the ALLPM (e.g. requested information, parameter update, low signal-level warning, occurrence of premature ventricular contraction, etc.) may be added. After an active communication window, all subsequent windows coinciding with the refractory period of the cardiac cycle are skipped to further reduce idle

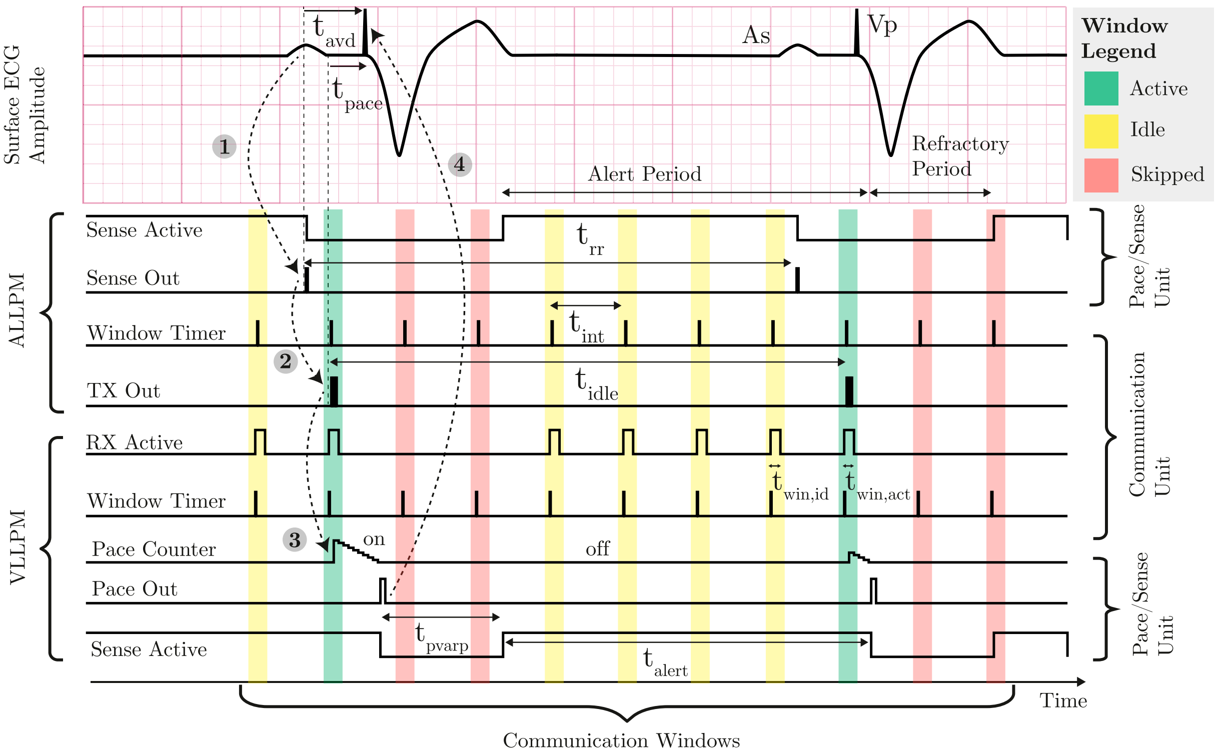


Fig. 2. Conceptual illustration of the proposed LLPM synchronization protocol based on SDC and typical event sequence in a cardiac cycle. Inter-device communication is restricted to brief periodic windows, spaced by t_{int}, and is always initiated by the ALLPM. Upon detection of a P-wave (event 1), the ALLPM wakes-up its transmitter in the next scheduled window (event 2) to send a pacing trigger and the corresponding delay t_{pace} to the VLLPM (event 3). Subsequently, the VLLPM will pace the right ventricle after t_{pace} seconds if no intrinsic QRS-wave is detected in the meantime (event 4). The ALLPM also acts as the system's timekeeper ensuring the correct window period and timing. Specifically, subsequent message transmissions are always spaced by an integer multiple of t_{int}, allowing the VLLPM to precisely synchronize its sleep/wake cycle to that of the ALLPM. To minimize idle listening time, all scheduled communication windows coinciding with the refractory period of the cardiac cycle are skipped. **Signal Legend:** *Sense Active* - On/off-state of ECG sense amplifier; *Sense Out* - Output of ECG sense amplifier, signalling detection of P-wave; *Pace Counter* - Counter triggering pacing pulse delivery upon completion; *Pace Out* - Output of pacing unit, i.e. pacing pulse; *Window Timer* - Output of sleep/wake timer implementing t_{int}-interval; *TX Out* - Output of synchronization transmitter; *RX Active* - On/off state of synchronization receiver.

listening time. Thus, the receiver's sleep time is temporarily extended to a multiple of t_{int} after receiving a pacing command as illustrated in Fig. 2.

Ensuring precise synchronization of the transceiver activation is crucial. The VLLPM's receiver must align its sleep/wake rhythm to that of the ALLPM's transmitter to prevent missing messages. It can achieve synchronization by inferring the correct timing from the received data, as consecutive messages from the ALLPM start at an integer multiple of t_{int}.

Based on these considerations, the optimum window period t_{int} is equal to the AV-delay. This enables beat-by-beat AV-synchrony even for high heart rate variability, with the minimum number of communication windows, and thus, receiver current consumption. Specifically, since the communication windows cover the entire alert period, the proposed synchronization approach can operate up to the maximum heart rate for which the LLPM has been programmed.

B. Receiver Duty-Cycle

Given the above described synchronization protocol, the subsequent section analyzes the minimum required receiver duty-cycle to guarantee AV-synchrony.

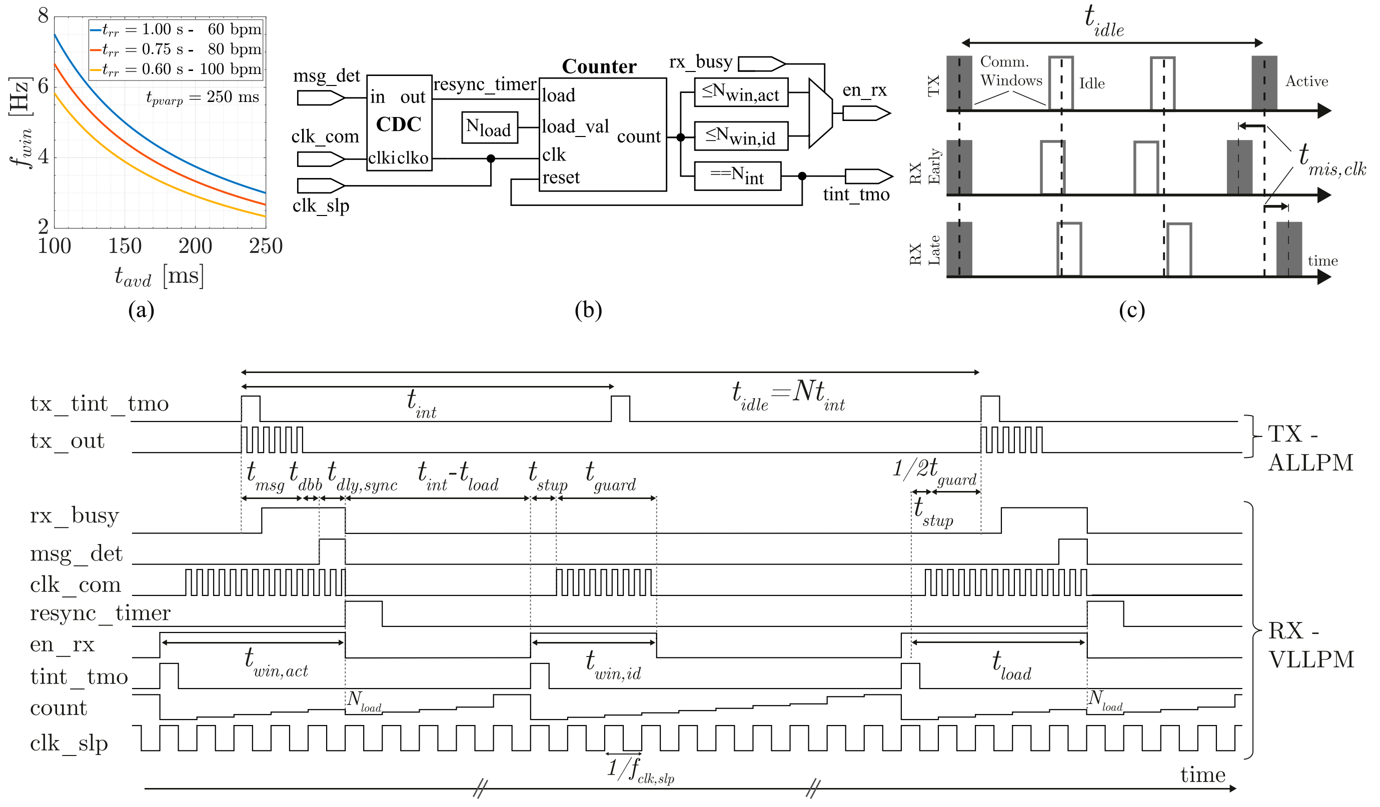
In contrast to the dual-receiver approach of [6], the proposed strategy uses a single duty-cycled receiver that is activated synchronously with the transmitter of the second device multiple times per cardiac cycle. Consequently, it is highly important to reduce the RX duty-cycle d_{rx} as much as possible to minimize the average current, given by

$$I_{rx,avg} = d_{rx} I_{rx,on} + (1 - d_{rx}) I_{rx,sleep}, \tag{1}$$

where $I_{rx,on}$ and $I_{rx,sleep}$ represent the current consumption during communication and sleep mode, respectively. In the subsequent analysis, only the receiver of the VLLPM is considered, since it has the larger duty-cycle of the two devices. Based on Section II-A and Fig. 2, the duty-cycle is given by,

$$\begin{aligned} d_{rx} &= f_{win,id} t_{win,id} + f_{win,act} t_{win,act} \\ &= (f_{win} - f_{win,act}) t_{win,id} + f_{win,act} t_{win,act} \end{aligned} \tag{2}$$

where $f_{win,id}$ and $f_{win,act}$ are the average frequencies of idle and active communication windows, respectively. In the second equation of (2), f_{win} represents the average frequency of both window types combined (i.e. $f_{win} = f_{win,id} + f_{win,act}$), which is further analyzed in Section II-C. Likewise, $t_{win,id}$ and $t_{win,act}$ in (2) are the duration of idle and active communication windows, respectively, which are defined and analyzed in detail in Section II-D.



(a) (b) (c)

(d)

Fig. 3. (a) Average RX window frequency, based on (3), as function of the AV-delay at three different heart rates. (b) Wake-up timer model used for analysis of minimum RX duty-cycle and t_{int} accuracy calculation based on the proposed LLPM synchronization protocol. (c) Drift of communication window timing between subsequent message transmissions due to RX/TX sleep clock frequency mismatch. (d) Timing diagram illustrating receiver operation under synchronous duty-cycling and re-synchronization of wake-up timer based on model in subfigure (b).

C. Window Frequency f_{win}

The window frequency f_{win} depends, in case of no skipped windows, solely on the AV-delay and is given by $f_{win,base} = 1/t_{avd}$ (i.e. window period t_{int} in Fig. 2 equals t_{avd}). Scheduled windows that fall into the refractory period can be skipped, reducing the window frequency to

$$f_{win} = f_{win,base} \frac{t_{alert}}{t_{rr}} = \frac{t_{rr} - t_{pvarp}}{t_{avd} t_{rr}}, \tag{3}$$

where t_{rr} is the heartbeat interval from R peak to R peak, and t_{pvarp} is the refractory period of the LLPMs after ventricular activation. Fig. 3(a) plots f_{win} as function of t_{avd} for three heart rates and a typical t_{pvarp} of 250 ms. As seen in the figure, only 4–6 windows per second would be required for typical pacemaker programming and an average heart rate of 60 bpm.

D. Window Duration

The second relevant factor influencing the receiver duty-cycle is the duration of each window, which can be split into either four or two main contributions, depending on whether or not a message is received during the given window (i.e. whether there is an active or idle window). The duration of idle windows is given by

$$t_{win,id} = t_{stup} + t_{guard}, \tag{4}$$

where t_{stup} and t_{guard} represent the startup time from sleep to active mode and the guard time, respectively, as explained in Sections II-D3 and II-D2. In contrast, active windows are extended by the message duration t_{msg} and the detection delay t_{det}, as explained in Section II-D1, i.e.

$$t_{win,act} = t_{stup} + t_{guard} + t_{msg} + t_{det}. \tag{5}$$

The subsequent analysis assumes a simple digital timer, clocked from a 32.8 kHz crystal oscillator, for generating the sleep/wake pattern of the receiver, based on the model shown in Fig. 3(b).

1) Message Duration & Detection Delay: The duration of a communication message is given by

$$t_{msg} = \frac{n_b}{f_{data}}, \tag{6}$$

where n_b and f_{data} are the number of bits per message and the data rate, respectively. The amount of information that needs to be exchanged between the devices is rather low for the given application, requiring only n_b = 10–30 bits per message [6]. Assuming a data rate in the range of 100–500 kb/s, which has previously been demonstrated as efficient for CIC, would result in an overall message length of $t_{msg} \sim$ 20–400 μs.

The detection delay t_{det} is the sum of the digital baseband latency t_{dbb} and the synchronization delay $t_{dly,sync}$ of the wake-up timer, i.e. $t_{det} = t_{dbb} + t_{dly,sync}$ (cf. Fig. 3(d)).

By optimizing the digital baseband circuits for minimum latency, t_{dbb} can in principal be reduced to 1–2 bit periods at the given data rate, thereby minimizing its impact on $t_{win,act}$. The synchronization delay $t_{dly,sync}$ is discussed in more detail in Section II-D2.

2) Guard Time: The proposed protocol relies on the precise alignment of the sleep/wake cycles of both devices, i.e. the synchronous activation of the transceivers during communication windows. As explained in Section II-A and shown in Fig. 3(d) based on the model in Fig. 3(b), the VLLPM uses each received message from the ALLPM to compensate for any temporal drift in the window synchronization that has built up since the previous message. However, as illustrated in Fig. 3(c) and 3(d), the achievable synchronization precision is restricted due to the frequency and phase mismatch of the devices' oscillators, which are used to measure the sleep interval. Firstly, as shown in Fig. 3(c), frequency mismatch can shift the start of the ventricular window symmetrically with respect to the atrial window by

$$t_{mis,clk} \in 2\frac{\Delta f_{clk,slp}}{f_{clk,slp}} t_{idle}\left[-1,1\right], \tag{7}$$

where $f_{clk,slp}$ and $\pm\Delta f_{clk,slp}$ represent the nominal value and the maximum deviation of the clock frequency, respectively, and t_{idle} is the time interval since the last re-synchronization, i.e. the last received atrial message. Secondly, since the oscillators of the two devices are not phase-locked, messages arrive asynchronously with respect to the receiver clock (cf. Fig. 3(d)), leading to a random synchronization delay in the range of one clock period, i.e.

$$t_{dly,sync} \in \left[0, T_{clk,slp}\right]. \tag{8}$$

The overall shift of the RX window timing is thus given by,

$$t_{shift} = t_{mis,clk} + t_{dly,sync}. \tag{9}$$

Therefore, to not miss any messages from the ALLPM, the receiver needs to be ready at $max(t_{shift})$ seconds before the expected start of the communication window and check for incoming data for at least,

$$\begin{aligned} t_{guard} &= max(t_{shift}) - min(t_{shift}) \\ &= 4\frac{\Delta f_{clk,slp}}{f_{clk,slp}} t_{idle} + T_{clk,slp}. \end{aligned} \tag{10}$$

Using a 32.8 kHz crystal oscillator, with a typical precision of ±20 ppm, to generate $f_{clk,slp}$ in both LLPMs and assuming $t_{idle} = 1.5$ s, results in $t_{guard} = 150\ \mu$s.

3) Startup Time: The startup time is the interval from the activation of the receiver's communication unit until data reception can start, which depends on the specific circuit implementation, but is typically limited by the settling of high-impedance nodes and low-frequency filters. A fast startup time is especially critical to minimize the window duration, since previous considerations have shown that the other contributors t_{guard} and t_{msg} are relatively brief (~100–200 μs each). In fact, even for an optimistic estimation of 10–20 bit periods at the anticipated data rate, t_{stup} considerably impacts the overall duty cycle. Thus, an essential aspect in the receiver design, presented in Section III, is to focus on reducing the startup time.

TABLE I
PROTOCOL AND CHANNEL PARAMETERS AFFECTING THE RX DUTY-CYCLE AND THE TX OUTPUT CURRENT

Parameter	Value	Description
t_{avd}	150 ms	AV-delay
t_{pvarp}	250 ms	Refractory period after ventricular activation
t_{rr}	1 s	Avg. RR-interval, i.e. inverse of heart rate
f_{hr}	60 bpm	Avg. heart rate
$f_{hr,max}$	150 bpm	Max. heart rate[a]
f_{win}	5 Hz	Avg. frequency of communication windows
$f_{win,act}$	1 Hz	Avg. frequency of active windows
t_{idle}	1.5 s	Max. time w/o communication
n_b	20 bits	Avg. number of bits per message
f_{data}	100 kb/s	Communication data rate
t_{msg}	200 μs	Duration of communication message
$f_{clk,slp}$	32.8 kHz	Frequency of sleep/wake timer
$\frac{\Delta f_{clk,slp}}{f_{clk,slp}}$	±20 ppm	Precision of sleep/wake timer
t_{guard}	150 μs	Min. time to wait for incoming data
G_{ch}	−66 dB	Worst-case intracardiac channel gain
$R_{el,tx}$	400 Ω	TX inter-electrode impedance

[a] The maximum heart rate, which a LLPM and the proposed synchronization approach can support, depends on t_{avd} and t_{pvarp}, with the upper limit given by $f_{hr,max} = \frac{1}{t_{avd}+t_{pvarp}}$ [10].

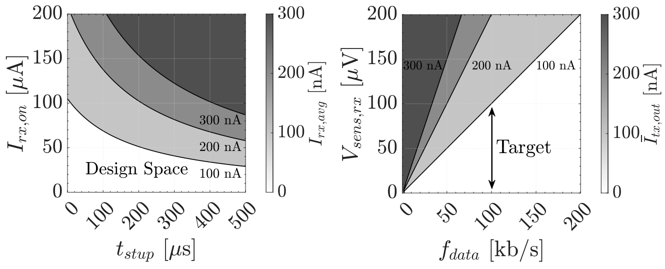
Table I provides a summary lists of all protocol parameters affecting the duty-cycle and their typical values based on the above considerations.

E. Implications for Receiver Design

The prior analysis allows to derive the requirements for the remaining key parameters influencing the average receiver current $I_{rx,avg}$, namely the startup time t_{stup}, the active current $I_{rx,on}$ and the sensitivity $V_{sens,rx}$. First, Fig. 4(a) plots the available design space in terms of t_{stup} and $I_{rx,on}$ for different targets of $I_{rx,avg}$ based on (1)–(10) and the values in Table I. Second, to derive a requirement for $V_{sens,rx}$, the average transmitter output current $\bar{I}_{tx,out}$ has to be considered, which is given by

$$\bar{I}_{tx,out} = I_{tx,out} t_{msg} f_{win,act} = \frac{V_{sens,rx}}{G_{ch} R_{el,tx}} \frac{n_b}{f_{data}} f_{win,act}, \tag{11}$$

where I_{tx} is the momentary output current during data transmission, G_{ch} the worst-case intracardiac channel gain and $R_{el,tx}$ the TX inter-electrode impedance. Fig 4(b) plots $\bar{I}_{tx,out}$ as function of f_{data} and $V_{sens,rx}$ for typical channel characteristics (i.e. $G_{ch} = -66$ dB and $R_{el,tx} = 400\ \Omega$) and the values in Table I. Since both the transmitter and receiver are part of a LLPM with a similarly limited battery capacity, their current consumption should be balanced to maximize the longevity of the entire dual-chamber system. Therefore, to achieve a 100 nA target for both $I_{rx,avg}$ and $\bar{I}_{tx,out}$ at $f_{data} = 100$ kb/s, $V_{sens,rx}$ should be below 100 μV, while t_{stup} and $I_{rx,on}$ should fall into the highlighted area in Fig. 4(a).



(a) (b)

Fig. 4. Allowable RX design space for different targets in (a) average RX current $I_{rx,avg}$ and (b) average TX output current $\bar{I}_{tx,out}$ based on duty-cycle analysis in (1)–(10) and Table I.

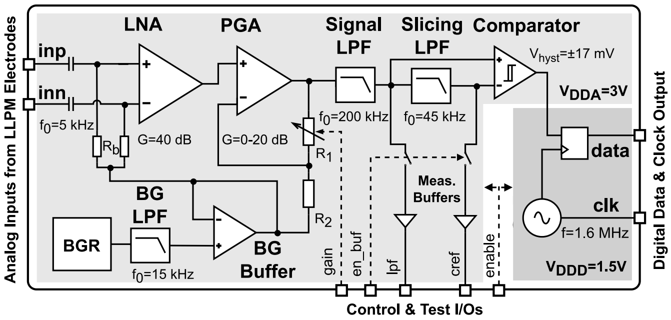


Fig. 5. Architecture of proposed direct-digital CIC-receiver ASIC.

III. Receiver Design

A. System-Level Considerations & Receiver Architecture

The proposed CIC-receiver adopts DDC with Manchester-encoded data to maximize energy efficiency. DDC reduces current consumption compared to modulation approaches using a high-frequency carrier, since power-hungry modulation/de-modulation circuits are avoided and the required receiver bandwidth only depends on the data rate. DDC is especially suited for intracardiac communication, which has a relatively flat channel frequency response and thus allows for distortion-free signal transmission without the need for equalizers [23]. Manchester-encoding has multiple system-level advantages due to being a self-clocking signal with zero DC component [32]. First, stronger high-pass filtering is possible, compared to NRZ/RZ-encoding, without considerably lowering the signal-to-noise ratio. This allows for faster receiver startup by increasing the bandwidth of DC biasing circuits, which usually limit the settling time. Second, the self-clocking feature allows for simple bit synchronization without relevantly increasing the packet length and relaxes the precision requirement of the RX oscillator. Third, an oversampling-based digital decoder for bit synchronization can be realized with only a few logic gates operating at low current consumption [33].

Fig. 5 shows the overall receiver architecture, operating at a target data rate of 100 kb/s. The signal-path is composed of two gain stages, a second-order low-pass filter (LPF) and a slicing comparator with internal hysteresis and an adaptive threshold. A 1.6 MHz oscillator is used to generate the clock for the (off-chip) digital circuits and to provide a synchronous signal output by sampling the comparator. The bias currents and voltages for each block are derived from an on-chip bandgap reference (BGR).

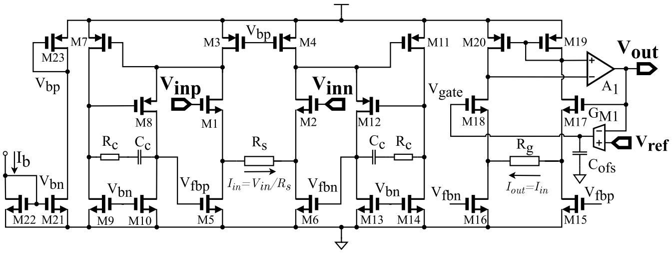


Fig. 6. Detailed LNA schematic with differential inputs and single-ended output. The gain is set by the resistor ratio R_g/R_s. The offset-compensation loop, formed by G_{M1}, C_{ofs} and M18, sets V_{gate} such that the DC level of V_{out} coincides with the reference voltage V_{ref}, which is provided by the on-chip bandgap reference.

The main architecture-level improvements over existing intra-body DDC receivers are as follows. First, the low-noise amplifier (LNA) features offset-compensation to accommodate larger system gain required for improving sensitivity. Second, adaptive biasing schemes are employed in low-frequency filters to significantly reduce settling times of high-impedance nodes at startup without sacrificing steady-state performance. Third, using a hysteresis comparator with adaptive threshold for bit slicing, allows to simultaneously improve SNR and startup speed.

B. Circuit Design

The differential inputs, connected to the pacemaker electrodes, are AC-coupled to remove any electrode offset and to provide a first stage of filtering. The cut-off frequency of the input high-pass filter (HPF) was set at 5 kHz, to prevent amplifier saturation due to the intrinsic electrical signals from the heart, which have dominant energy contents at frequencies below 50 Hz and maximum transient amplitudes of a few ten millivolts [34].

Fig. 6 shows a detailed schematic of the LNA, which provides a fixed gain of 40 dB, differential to single-ended conversion and offset-compensation. The architecture is based on previous designs of current-feedback instrumentation amplifiers for biosignal and bioimpedance sensing, but has been modified to improve the startup time [35], [36].

The operation principle of the LNA is as follows. The drain currents of M1 and M2 are maintained equal in the presence of a small input signal ($V_{in} = V_{inp} - V_{inn}$) by the two feedback amplifiers formed by M7-M10 and M11-M14, respectively. Thus, V_{in} appears directly across the resistor R_s, which results in a differential current between M5 and M6, given by $\Delta I = 2I_{in} = 2V_{in}/R_s$. The current ΔI is mirrored via M15 and M16 to the output section of the LNA, which effectively is a copy of the input section. Likewise, as the drain currents through M17 and M18 are kept constant and equal by the feedback amplifier A_1, the differential current between M15 and M16 has to flow through resistor R_g. In the frequency range of the signal, the gate voltage, and thus also the source voltage, of M18 can be regarded as ac-grounds. Thus, the ac-voltage across R_g appears directly at the gate of M17, the output voltage of the LNA, resulting in a signal gain of $V_{out}/V_{in} = R_g/R_s$.

As low-power operation is one of the most important requirements of the receiver, optimizing the noise performance of the LNA is key. Taking into account only the most dominant noise sources, the input-referred noise power density based on Fig. 6 is given by,

$$\overline{v_{ni,LNA}^2} = 2\overline{v_{ni,M1}^2} + \overline{v_{n,R_s}^2} + 2H_b^2(s)\overline{v_{n,R_b}^2} + 2\frac{g_{m,M3}^2}{(g_{m,M1}//2g_{m,R_s})^2}\overline{v_{ni,M3}^2} + \frac{g_{m,M5}^2}{g_{m,R_s}^2}\overline{v_{ni,M5}^2} + \overline{v_{n,R_{el}}^2}, \tag{12}$$

where $g_{m,M1}$, $g_{m,M3}$, $g_{m,M5}$ are the transconductances of the transistors M1/M2, M3/M4 and M5/M6, respectively, and $g_{m,R_s} = \frac{1}{R_s}$ and R_{el} the inter-electrode impedance arising due to the cardiac tissue and blood. Noise from the bias resistors R_b is low-pass filtered by,

$$H_b(s) = \frac{2 + R_{el}C_{in}s}{(2R_b + R_{el})\, C_{in}s + 2}, \tag{13}$$

where C_{in} represents the input capacitor. To minimize the noise contribution from R_b for a given cut-off frequency of the input HPF, C_{in} should be set to the maximum allowable value limited by either area constraints or the condition $R_b >> R_{el}$ to ensure a sufficiently high input resistance. To minimize the contributions from the current sources M3/M4 and the current mirrors M5/M6, their transconductances were reduced to the extent permitted by the available voltage headroom within the target supply voltage range of 2.4–3.3 V. In addition, $g_{m,M1}$ was maximized, by operating M1/M2 in weak inversion, as this simultaneously reduces noise contributions from M1-M4. Lastly, R_s was minimized within the bandwidth and stability constraints at the target LNA current, to reduce its noise and suppress contributions from M3-M6. Specifically, the differential and common-mode loop gain in the input stage (M1-M14) have the same dominant pole, defined by the Miller compensation network (C_C &R_C). However, the DC gain for a common-mode excitation is higher, since R_s does not act as a load for M5/M6 (in parallel to $g_{m,M1}/g_{m,M2}$), i.e. R_s is effectively an open-circuit. Thus, the unity-gain bandwidths of the two loops differ proportionally to their DC gain ratio, which increases with decreasing R_s. Consequently, R_s was minimized, while keeping both loops stable and ensuring sufficient closed-loop bandwidth for the differential signal.

The offset-compensation loop, comprising G_{M1}, C_{ofs} and M18, regulates V_{gate} to match the DC level of V_{out} to the reference voltage V_{ref}, provided by the on-chip BGR. Since the settling time of the LNA is limited by the offset-compensation loop, an adaptive biasing scheme is used for the transconductance amplifier (OTA) G_{M1} to prevent slewing at startup. A detailed schematic of G_{M1}, based on [37], is shown in Fig. 7. The circuit comprises two sections: transistors M1-M10 form a basic wide-swing OTA, while transistors M11-M22 increase the bias current based on the absolute level of the differential input voltage. As shown in [37], for input voltages below approximately $\frac{1}{2}V_T = \frac{kT}{2q}$, the additional tail current sources M18 and M19 are off and the circuit behaves as a standard OTA. This mode of operation occurs after receiver startup, since the signal swing on the output voltage of the LNA is below 10 mV$_\mathrm{p}$ for the target sensitivity. In contrast, during the startup phase, when the OTA encounters initially large input voltages, M18 and M19 are activated, substantially increasing the total bias current by several times the constant bias current I_b. After startup, G_{M1} and C_{ofs} in Fig. 6 form a first-order LPF with a cut-off frequency of 8 kHz. The bandgap (BG) LPF in the biasing branch in Fig. 5, which is also realized as a first-order g$_m$C-filter, uses the same adaptive OTA topology, to simultaneously accelerate the settling time of the bias voltages of the LNA and the programmable gain amplifier (PGA) during startup.

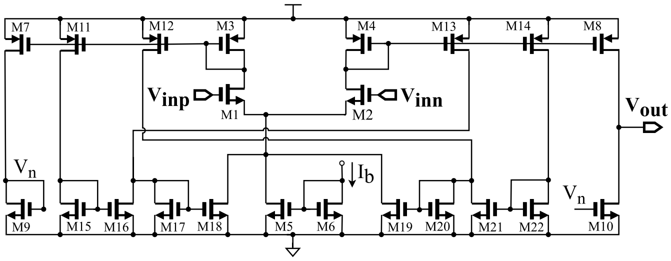


Fig. 7. Schematic of adaptive-biasing OTA.

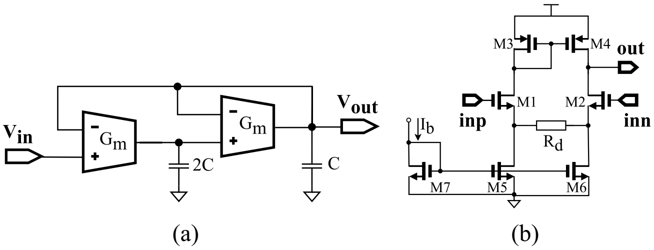


Fig. 8. (a) Schematic of second-order signal LPF and (b) implementation of G$_m$-cell.

The PGA uses a standard two-stage opamp and a variable feedback resistor R_1 to set four different gains in the range from 0–20 dB. To reduce current, the lower terminal of resistor R_2 is connected to a filtered and buffered version of the bandgap voltage, which coincides with the DC-level at the positive PGA input.

The signal LPF, shown in Fig. 8(a), was realized as a second-order g$_m$C filter with a cut-off frequency set at 200 kHz, since most of the energy in the PSD of a Manchester code is contained within a bandwidth up to the first zero, which occurs at twice the data rate frequency [32]. The two G$_m$-cells in Fig. 8(a) were realized as differential MOS-transconductors with resistive source degeneration, shown in Fig. 8(b), to ensure linear operation up to a maximum signal swing of 340 mV$_\mathrm{pp}$.

Fig. 9 shows the schematic of the comparator, which is composed of an open-loop two-stage opamp with internal positive feedback for hysteresis [38]. The switching thresholds were set at $V_{thr} = \pm 17$ mV to be above the RMS-noise level present at the comparator input. Consequently, the comparator only starts toggling once there is incoming data and thus also works

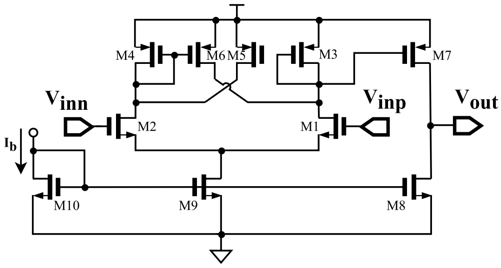


Fig. 9. Schematic of comparator with internal hysteresis, which is set by size ratios of M5/M3 and M6/M4.

as a signal detector. Depending on the specific requirements, the threshold-to-noise ratio can be adjusted from $\sim$2–20 by varying the PGA gain. The reference voltage, applied at the negative input of the comparator, is obtained by low-pass filtering the communication signal. This ensures optimal slicing performance since the DC levels of the two inputs match and track each other over variations in process parameters, supply voltage and temperature. Considering the differential comparator input, the slicing LPF thus effectively acts as an additional HPF on the signal with the same cut-off frequency. The HPF cut-off frequency has been set at a relatively high value of 45 kHz, since comparator hysteresis allows to aggressively high-pass filter the input signal, while at the output the original rectangular waveform of the transmitted signal is still faithfully recovered. In addition, increasing the HPF cut-off frequency also improves the startup time of the receiver. Specifically, the differential input voltage of the comparator settles faster to its steady-state value, i.e. the DC-offset, which is the critical criterion that the receiver is ready to receive data.

For clock generation, a state-of-the-art differential RC ring oscillator using five low-voltage delay stages based on [39] was implemented. The oscillator frequency was set at 1.6 MHz to provide a x16 oversampling clock for the off-chip digital Manchester decoder.

To facilitate duty-cycled operation, the biasing circuits of each block were implemented with enable/disable switches controlled by a single digital enable signal.

IV. Implementation Results

A. Electrical Performance

The proposed CIC-receiver was designed and implemented in a 180 nm CMOS process. Fig. 10(a)–10(c) show the measured gain, noise and startup characteristics, respectively, which were obtained from five different test samples.

All measurements were taken differentially at the input of the comparator using a PGA gain of 14 dB. The simulations, displayed alongside the measurements in Fig. 10(a)–10(c), were performed on the layout-extracted netlist of the receiver using typical corner models for all primitive devices. The measured receiver samples achieve a peak gain of 53.3 ± 0.1 dB (mean $\pm$ standard deviation), an output and input RMS noise level of 4.69 ± 0.13 mV and 10.1 ± 0.4 μV, respectively, with a current of 39.1 ± 0.6 μA. In addition, the receiver starts up in less than 250 μs, which is demonstrated by the transient comparator offset dropping considerably below the noise level within that time period after circuit activation (cf. Fig. 10(c)).

B. Communication Performance

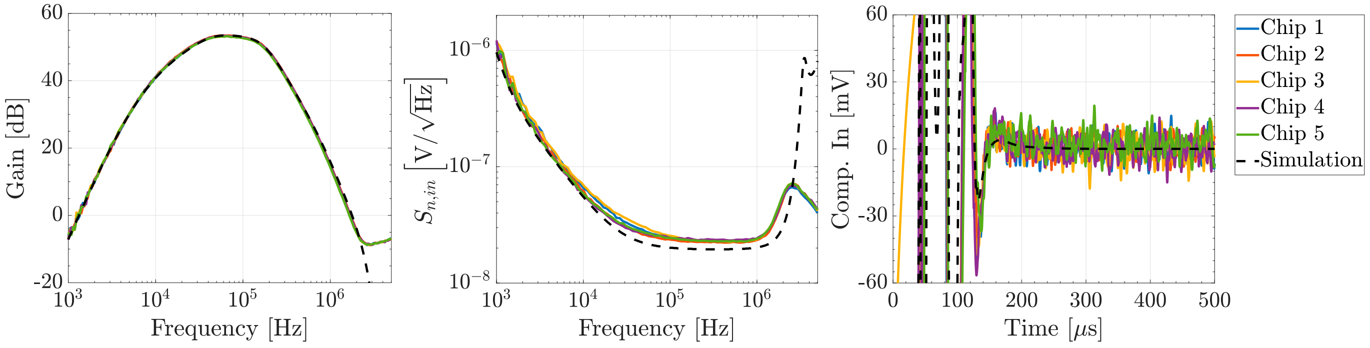
The receiver sensitivity was determined by measuring the packet-error-rate (PER) as function of the input amplitude, using the setup shown in Fig. 11(a). To this end, the RX output signal was demodulated off-chip by a digital Manchester decoder based on midbit-detection as in [33]. The decoder was implemented on a Zynq-7020 FPGA and uses a x16 oversampling clock provided by the 1.6 MHz oscillator from the receiver chip. To generate the input signal and record the demodulated baseband bit-stream, an Analog Discovery 2 device from Digilent was used. Since previous work demonstrated a relatively flat frequency response for the intracardiac channel, the channel was modeled with a attenuation network consisting of four resistors [20], [21], [23]. The resistors were dimensioned to achieve a typical LLPM inter-electrode impedance of 400 Ω and channel attenuation of 60 dB [9], [20], [21], [23]. In Fig. 11(b), the PER measurements of the five test samples are compared to a simulation based on typical receiver characteristics for a packet length of 32 bits. The PER simulation was performed in Simulink (MathWorks, USA) using a high-level RX model, based on the transfer function and noise spectrum obtained from prior transistor-level simulations. For a PER of 1e-3, the measured sensitivity is 81.6 ± 7.4 μV, whereas the expected value from simulation is 62 μV. This degradation in the measured sensitivity is mainly caused by the the increased noise level, observed in the previously reported electrical measurements (cf. Fig. 10(b)).

In addition to Fig 10(c), the receiver startup time was also more directly measured based on PER performance. To this end, the receiver was turned off in between two data packets, which were sent at an interval of 150 ms. The receiver was then activated t_{stup} seconds before the start of the next packet. Fig. 11(c) shows the measured PER as function of t_{stup}, indicating that the receiver settles rapidly and reaches steady-state performance around 160–200 μs after activation.

In summary, Table II lists the measured CIC-receiver performance alongside a breakdown of the current consumption, while Fig. 12 shows a micrograph of one of the test chips. With an active circuit area of 0.76 mm^2, the receiver could be readily accommodated in a contemporary LLPM housing, which typically has a cylindrical shape with a diameter of $\sim$6.5 mm and length of 32–38 mm [13].

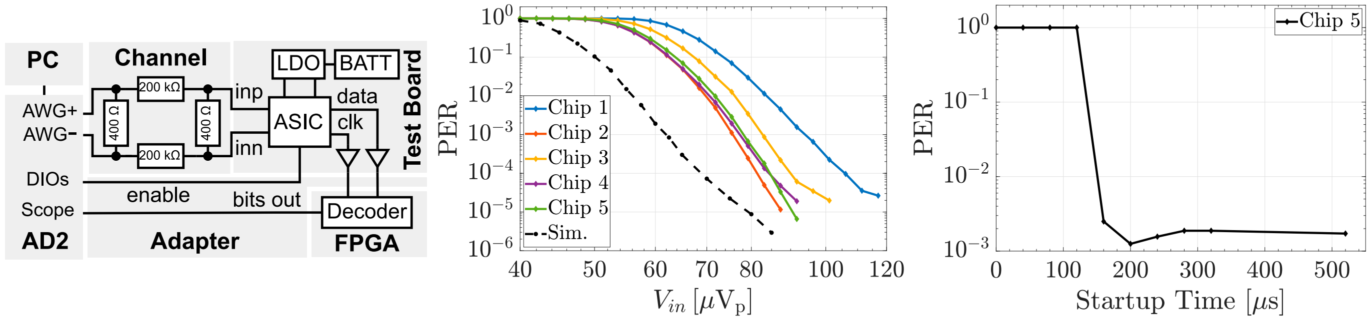
C. Duty-Cycled Activation - Average RX Current

Fig. 13(a) depicts the experimental setup used to assess the receiver performance when operated as specified by the proposed LLPM synchronization approach. Since the receiver design of this work focuses on the analog front-end, the necessary digital circuits for message detection, window timing generation and sleep/wake control were implemented on an FPGA (Zynq-7020). The sleep/wake controller and the wake-up timer operate from a 32.8 kHz clock from an external crystal oscillator



(a) (b) (c)

Fig. 10. Measured receiver characteristics are compared to a typical simulation. (a-b) Gain and input-referred noise density versus frequency. (c) Settling behavior of transient offset during startup after receiver has been activated at $t = 0$.



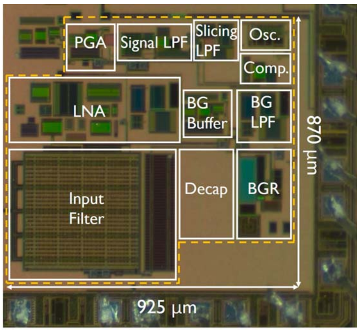
(a) (b) (c)

Fig. 11. (a) PER measurement setup. (b) Measured PER vs. receiver input amplitude V_{in}. (c) Measured PER as function of startup time, defined as the time span from receiver activation until packet start.

TABLE II
RECEIVER PERFORMANCE SUMMARY AND CURRENT BREAKDOWN

Performance Summary		Current Breakdown	
Parameter	**Value**	**Block**	**Sim/Meas.**^{a} **[μA]**
Technology	180 nm CMOS	LNA	21.6/-
Area	0.76 mm^2	PGA	4.0/-
Modulation	Direct-digital	BG Buffer	2.2/-
Line Code	Manchester	Signal LPF	3.4/-
Frequency	5–200 kHz	Comparator	2.6/-
Data Rate	100 kb/s	BGR	4.5/-
Supply Voltage	3/1.5 V	BG/SL. LPF	0.6/-
Sensitivity	81.6±7.4 μV$_p$	Total @ 3V	38.7/34.8±0.6
PER	1e-3 (32b/pkt)	Osc. @ 1.5V	5/4.3±0.1
Startup Time	<250 μs	**Total**	**43.7/39.1±0.6**

[a] Since all blocks per voltage domain are connected to the same supply, only the total current can be measured.



(a)

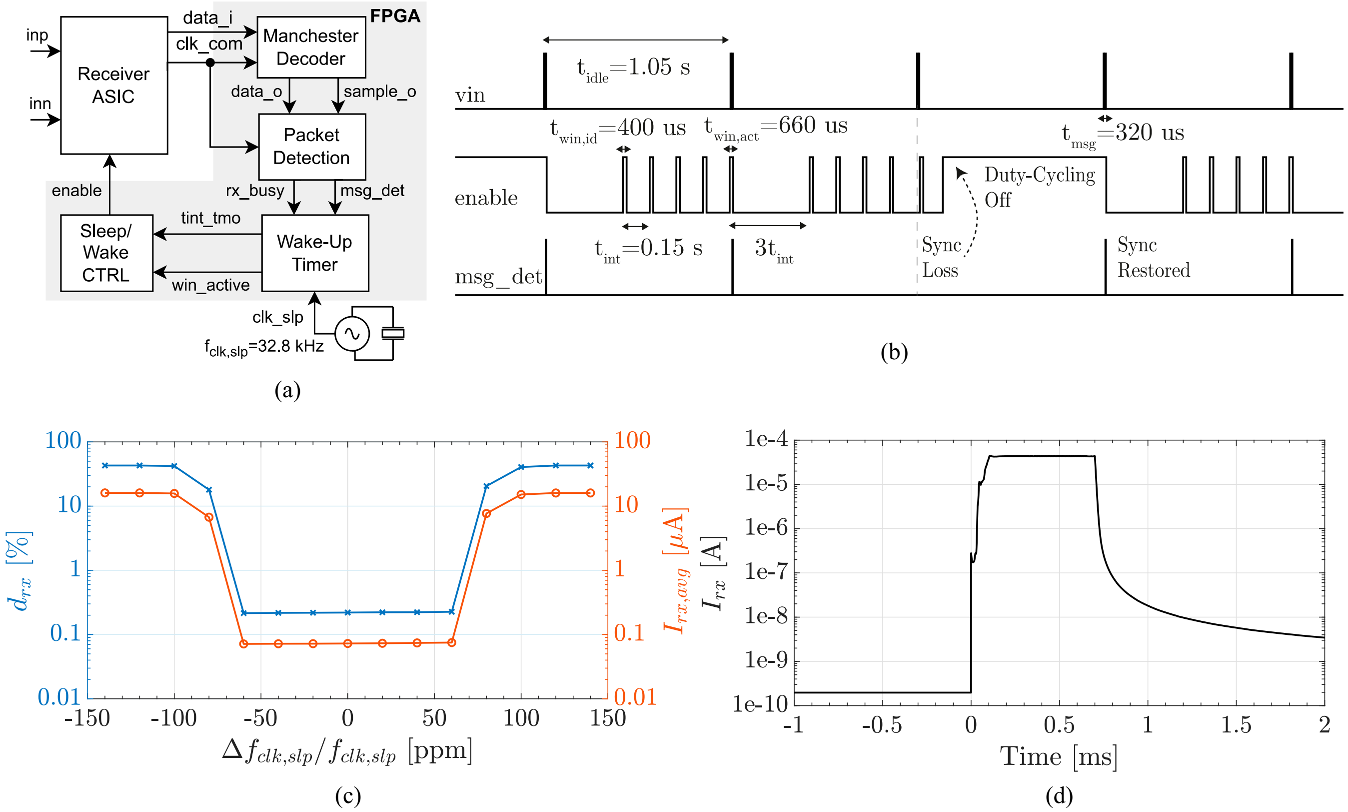
Block	Area [mm^2]
Input Filter	0.21
LNA	0.12
PGA	0.04
BG Buffer	0.09
Signal LPF	0.03
Slicing LPF	0.02
Comparator	0.02
BGR	0.04
BG LPF	0.03
Oscillator	0.02
Total	**0.76**

(b)

Fig. 12. (a) Die micrograph. (b) Circuit area split-up.

to enable and disable the rest of the receiver in synchrony with the transmitter's communication windows as described in Section II. The wake-up timer was implemented based on the model presented in Fig. 3(b).

The nominal window interval t_{int} was set at 150 ms and the transmitter would send one data packet every seventh window ($t_{idle} = 7 * t_{int}$), to mimic typical pacemaker operation at a heart rate of 57 bpm. Thus, the receiver is briefly activated every t_{int} seconds to check for incoming data. After each successfully received packet the sleep time would be momentarily increased to $3 * t_{int}$ (i.e. two skipped communication windows), to account for the refractory period after ventricular excitation, during which no communication is required. As illustrated in Fig. 13(b), if no packet is correctly received within t_{idle} seconds of the previous packet, the sleep/wake controller assumes loss of synchronization and activates the receiver continuously until



(a) (b) (c) (d)

Fig. 13. (a) Digital block diagram for functional implementation of proposed LLPM synchronization approach based on synchronous duty-cycling. (b) Conceptual illustration of receiver operation and relevant protocol timings. (c) Measured receiver duty-cycle and average current as function of TX/RX frequency mismatch of wake-up timer. (d) Simulated receiver current profile during duty-cycled operation. The enable signal is asserted and deasserted at $t = 0$ ms and $t = 0.7$ ms, respectively.

the next packet is detected. The receiver performance under synchronous duty-cycling was evaluated as function of the RX/TX sleep timer clock mismatch, defined as

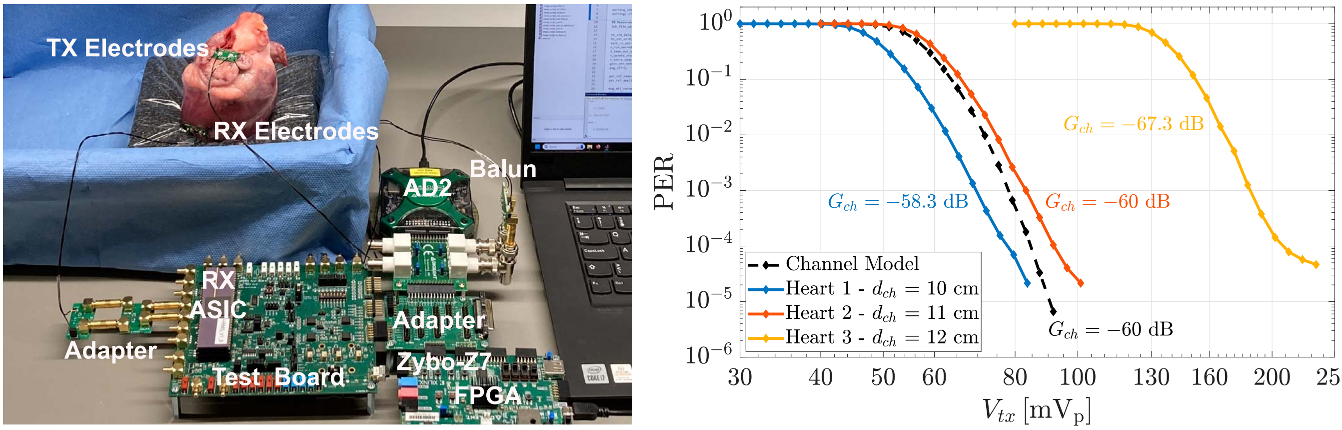
$$\frac{\Delta f_{clk,slp}}{f_{clk,slp}} = \frac{t_{int,rx} - t_{int,tx}}{t_{int,rx}}, \tag{14}$$

where $t_{int,tx}$ and $t_{int,rx}$ represent the effective window intervals generated at the transmitter and the receiver side, respectively. To this end, the transmitter window interval $t_{int,tx}$ was swept around the nominal value $t_{int,rx} = 150$ ms to cover a frequency mismatch range of ±140 ppm. Fig. 13(c) shows the resulting average duty-cycle and current consumption versus $\Delta f_{clk,slp}/f_{clk,slp}$ for a total measurement duration of 5 minutes per point. The receiver achieves a minimum duty-cycle of 0.22%, which reduces the average current to only 73 nA. The receiver does not experience any relevant transient current spikes at startup or turn-off, since the measured average current is below the product of the active current and the duty-cycle, i.e. $I_{rx,avg} < d_{rx} I_{rx,on}$. This is also indicated by the simulated current profile, shown in Fig. 13(d), which displays rapid onset and turn-off with no notable overshoot.

Lastly, Fig. 13(c) also demonstrates that the proposed synchronization approach works over a ±60 ppm range of frequency mismatch. This is well above the ±40 ppm worst-case mismatch of two standard-precision 32.8 kHz crystal oscillators assumed for the calculation of the minimum duty-cycle in Section II-B.

D. In-Vitro Validation

To validate the receiver performance in an environment mimicking the target setting, in-vitro measurements were conducted on porcine hearts freshly obtained from the slaughterhouse. Two pairs of needle electrodes, one on the right atrium and one on the right ventricle, were sutured epicardially to simulate a typical dual-chamber LLPM configuration. The same experimental setup as for the PER measurements in Section IV-B (cf. Fig. 11(a)) was used, except for two modifications. First, the transmitter (AD2 device) and the receiver were connected to the atrial and ventricular electrodes, respectively, rather than to the channel model. Second, to ensure galvanic isolation, a balun was inserted before the transmitter electrodes and the receiver outputs (signal and clock) were passed through an optocoupler before being connected to the FPGA. Fig. 14(a) shows a photo of the measurement setup. Fig. 14(b) plots the measured PER as function of the transmitter output voltage for three different hearts and electrode separations. The in-vitro measurements closely match those obtained from the channel model, suggesting that the selected channel model was appropriate for evaluating the receiver performance in previous sections. Lastly,



(a) (b)

Fig. 14. (a) Photograph of the setup used for in-vitro PER measurements on porcine hearts. (b) PER vs. transmitter amplitude V_{tx} for three different hearts and TX/RX separations d_{ch}. Channel gains G_{ch} were measured at 100 kHz prior to the PER experiments.

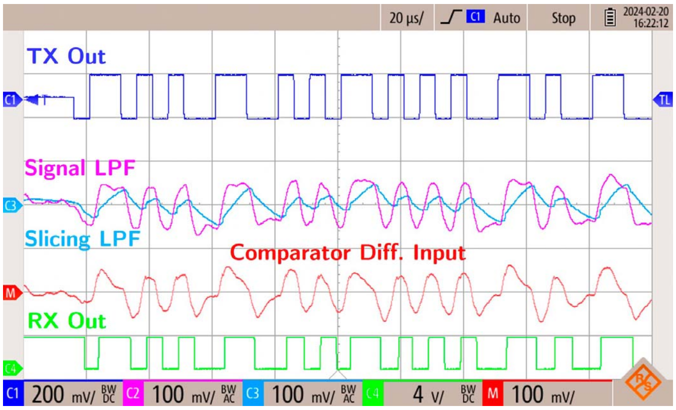


Fig. 15. Transient receiver waveforms measured during in-vitro experiments.

Fig. 15 shows the transient waveforms measured at the comparator input and output during one of the in-vitro experiments.

V. DISCUSSION

A. Receiver ASIC - State-of-the-Art Comparison

Table III compares the proposed receiver to previous state-of-the-art designs for low-power intra-body communication. The energy-efficiency for steady-state operation of different implementations is evaluated by a commonly used Figure-of-Merit (FoM), defined as,

$$FoM = 10\log_{10}\left(\frac{f_{data}}{P_{rx}P_{sens}}\right), \tag{15}$$

where f_{data}, P_{rx} and P_{sens} represent the data rate, the power consumption and the sensitivity, respectively [40], [41]. This work has one of the highest FoMs among previous intra-body sub-mW receivers, although featuring fully differential inputs and including the current consumption for on-chip bias generation and frequency synthesis. However, the main improvement over existing literature is the receiver's rapid startup time, which enables highly duty-cycled operation. This is beneficial for applications, which simultaneously require ultra-low-power operation and high energy-efficiency. Specifically, Fig. 16 evaluates energy-efficiency compared to previous work in the context of LLPM synchronization. To this end, the average receiver current consumption $I_{rx,avg}$ is plotted against the estimated transmitter output current $\hat{I}_{tx,out}$ for a typical communication scenario where one message of 32-bits is transmitted every second. The transmitter output current was calculated based on (11), using the reported values in Table III for receiver sensitivity and data rate and a typical intracardiac channel attenuation of 66 dB and inter-electrode impedance of 400 Ω [9], [20], [21], [23]. As demonstrated in Fig. 16, the presented duty-cycled receiver allows for a 2–3 order of magnitude improvement in synchronization current consumption compared to previous receivers targeted for continuous operation. In addition, the receiver of this work supports sporadic short-packet communication. In fact, due to using Manchester-encoding only two overhead bits per message are required for packet synchronization. In contrast, implementations based on NRZ/RZ-encoding and CDR RX architectures, such as [24], [25], [26], [28], require substantially longer synchronization headers, which easily double or triple the total number of bits per packet for small payloads of only 10–30 bits.

B. LLPM Synchronization - System Current Consumption

At this stage, the overall receiver current consumption to perform LLPM synchronization based on the proposed approach cannot be directly determined, since the presented ASIC is missing the digital baseband (DBB) circuitry and the wake-up timer to control the sleep/wake pattern of the communication circuits. However, those blocks can be implemented, if integrated alongside the existing circuits in a future chip, at extremely low current levels. First, recent DBB receivers, using oversampling-based Manchester demodulation, have achieved a current consumption of 1 μA and 7 μA for data rates of

TABLE III
PERFORMANCE COMPARISON WITH PREVIOUS INTRABODY COMMUNICATION RECEIVERS

Publication	H. Cho JSSC '16 [42]	S. Maity JSSC '19 [26]	J. Park JSSC '19 [43]	B. Yuk SSC-L '20 [27]	S. Maity JSSC '21 [24]	B. Chatterjee ISSCC '22 [28]	N. Modak JSSC '22 [25]	This Work[a]
CMOS Process [nm]	65	65	65	110	65	65	65	180
Area [mm^2]	0.17[b]	0.12	0.10	0.22	0.09	0.12	0.04	0.76
Frequency [MHz]	13.56	0-30	37.5-42.5	0-20	1	0-20	1	0.005-0.2
Data Rate [Mb/s]	0.1	30	5	16.7	0.01	15	0.02	0.1
Modulation	OOK	Direct Digital	OOK	Direct Digital	OOK	Direct Digital	OOK	Direct Digital
Line Code	NRZ	Polar NRZ	NRZ	Polar RZ	NRZ	RZ-CPPM	NRZ	Manchester
Supply Voltage [V]	0.8	1	0.6	3.3/1	0.7	0.75	0.5	3/1.5
RX Current [μA]	53.1[c]	98	39.2	62.3	2.07[d]	80.8	0.388[d]	39.1 ± 0.6
RX Power [μW]	42.5[c]	98	23.5	62.3	1.45	60.6	0.194	111 ± 2
BER	1e-5	1e-3	1e-3	1e-9	1e-3	1e-3	1e-3	1e-3[f]
Sensitivity [mV$_\mathrm{p}$]	0.316	3.21	3.97	4.50	0.224	10	0.562	0.082 ± 0.007[f]
Sensitivity [dBm][e]	-60	-37	-41	-34	-63	-30	-55	-69 ± 1
Startup Time [μs]	-	-	-	-	-	-	-	<250
On-Chip Bias/Osc.	no/(yes)[c]	no	no/yes	no/yes	no	no/yes	no/yes	yes
Fully-Differential Input	no	no	no	yes	no	no	no	yes
Suited for Short-Packet Comm.	yes	no[g]	yes	yes	no[g]	no[g]	no[g]	yes
FOM[h]	184	182	184	178	191	174	195	188 ± 1

[a] Measurement results specified as mean ± standard deviation.

[b] Including TX area.

[c] Unclear from [42] if consumption from 40 MHz crystal-oscillator for system clock is included in RX current.

[d] Sum of standby and active current.

[e] For a 50 Ω input impedance.

[f] Sensitivity is reported for PER=1e-3 based on Table II, i.e. assuming worst-case conversion from PER to BER.

[g] Large sync bit overhead for payloads of only 10–30 bits, due to CDR-based RX architecture.

[h] $FoM = 10\log_{10}\left(\frac{f_{data}}{P_{rx}P_{sens}}\right)$, based on rows 5, 10 & 13.

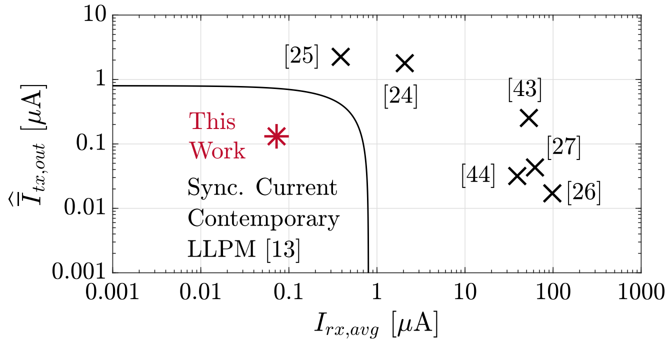


Fig. 16. Performance comparison with previous intra-body receivers in the context of LLPM synchronization based on average receiver current $I_{rx,avg}$ and average transmitter output current $\hat{\bar{I}}_{tx,out}$ (cf. main text for a detailed explanation of the considered scenario and calculation). The solid line is defined by $I_{rx,avg}+\hat{\bar{I}}_{tx,out} = 800$ nA, reflecting the synchronization current consumption of contemporary dual-chamber LLPMs, which is 800 nA under default settings [13].

40 kb/s and 250 kb/s, respectively [44], [45]. Assuming a similar DBB architecture was adopted for LLPM synchronization and the same duty-cycle applies as for the analog front-end (cf. Fig. 13(c)), the contribution of the DBB to the average RX current would be less than ∼20 nA. Second, it has been demonstrated that accurate timers based on 32.8 kHz quartz crystal oscillators can be realized at current levels below 50 nA, including the consumption of oscillator core, bias circuits, clock dividers and control logic to implement variable sleep intervals [29], [30], [31].

For a complete estimation of the transceiver current consumption, the transmitter also needs to be considered. Typically, the TX current is dominated by the output stage, which needs to provide sufficient power for the given channel attenuation and RX sensitivity. Using (11), the average output current is estimated to be $\bar{I}_{tx,out} = 82$ nA, taking into account both the communication parameters listed in Table I and the measured receiver performance (cf. Table II).

Therefore, based on the results of this and earlier work, an average transceiver current of 300-400 nA seems achievable with the proposed LLPM synchronization approach, which would represent a factor x2–2.5 improvement compared to the transceivers in [8]. This is very promising for prolonging device longevity and potentially also reducing the number of re-interventions. From a clinical perspective, this would bring significant advantages, including fewer complications and decreased treatment costs.

C. Limitations

The presented work has a few limitations. The duty-cycled protocol imposes constraints in terms of bi-directional communication, latency and maximum data rate. Although communication from the ALLPM to the VLLPM is prioritized, the VLLPM can still transmit data in every cardiac cycle, directly after it has received a message from the ALLPM. In addition, communication beyond beat-by-beat P-wave synchronization, which is fully supported, is comparatively rare and not severely limited by these constraints. For instance, time-varying parameters like minimum maintained heart rate, which may also require synchronization across devices, change on time scales of several seconds to minutes [10]. Thus, the time interval between parameter updates is typically much longer than the worst-case latency imposed by the protocol, which is on the order of one cardiac cycle (cf. Section II). Additionally, parameter synchronization may intermittently increases communication load by a few dozen bits, which can be readily accommodated with the given data rate of 100 kb/s.

The proposed synchronization approach relies on an accurate timer to generate the sleep/wake cycles, the implementation of which was beyond the scope of of this work. However, the results presented for the minimum achievable receiver duty-cycle and average current, shown in Fig. 13(c), were obtained with sufficiently extended listening times per window, accommodating worst-case scenarios for timer frequency accuracy and synchronization error based on the assumptions in Section II-B. As discussed in Section V-B, integrating the timer on the same chip, following state-of-the-art designs, is not expected to prohibitively increase the overall current consumption. Additionally, sharing the required oscillator with other LLPM circuitry would further mitigate the impact on system current. Specifically, contemporary dual-chamber LLPMs have a total current consumption of 1.75 μA, with the synchronization transceiver consuming 800 nA, under default settings and without pacing [13].

The receiver performance could not be evaluated in an in-vivo configuration, as this would have required the implementation of a complete endocardial LLPM prototype, which was beyond the scope of this work. However, the presented receiver results obtained during in-vitro experiment on porcine hearts are promising. On the one hand, previous studies have demonstrated that the time-averaged channel characteristics observed in in-vivo porcine hearts reasonably agree with those measured in in-vitro environments [23], [46]. On the other hand, the time-variation of the channel attenuation caused by the heartbeat are not expected to significantly change the presented results. This is due to cardiac motion happening on a much slower time scale compared to LLPM synchronization, effectively making the channel attenuation constant over the duration of a typical message considered here.

D. Future Work

This work suggests a valuable approach towards reducing the synchronization current consumption of future LLPMs. Therefore, the authors aim to combine the presented receiver with the remaining state-of-the-art circuitry to realize a complete LLPM implant. A fully integrated system would enable precise assessment of the power-saving potential of the presented approach in a realistic in-vivo environment. In addition, the future receiver design targets several areas of improvement. These include investigating alternative circuit topologies to lower active current consumption, optimizing compensation networks to enhance settling speed during startup, and exploring adaptive window timing strategies to actively compensate for TX/RX frequency mismatch. These efforts could further reduce the duty-cycle and average current consumption of the system, but were beyond the scope of this work.

VI. CONCLUSION

This work presents both a power-optimized strategy for LLPM synchronization based on synchronous transceiver duty-cycling and a novel low-power CIC-receiver optimized for fast startup and sporadic short-packet communication. A direct-digital communication approach with Manchester-encoding operating at a data rate of 100 kb/s was adopted. The receiver achieves a sensitivity of 81.6 ± 7.4 μV with a current of 39.1 ± 0.6 μA and a startup time below 250 μs. Operating the receiver according to the proposed synchronization protocol, a duty-cycle of 0.22% would be required to achieve AV-synchrony for typical LLPM programming, resulting in a measured average current of only 73 nA. In conclusion, this work indicates that employing synchronous duty-cycling for CIC-based implant synchronization is highly promising to considerably reduce the current consumption of today's state-of-the-art dual-chamber LLPMs. Consequently, device longevity may be increased, potentially reducing the frequency of costly and complication-prone re-interventions.

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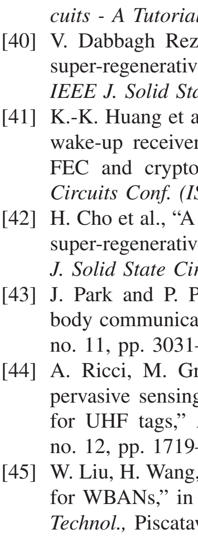

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